In the Claims:

Claim 1 (currently amended): A method comprising steps of:

receiving a plurality of parameter values for a multi-component circuit having at least one subcircuit model, said plurality of parameter values comprising at least a slice parameter value, said plurality of parameter values determining a plurality of parasitic values of said multi-component circuit;

generating a layout of said multi-component circuit utilizing said plurality of parameter values, said layout causing said multi-component circuit to have said plurality of parasitic values.

Claim 2 (original): The method of claim 1 further comprising a step of utilizing said plurality of parasitic values to simulate an electrical behavior of said multi-component circuit prior to said generating step.

Claim 3 (original): The method of claim 1 wherein said plurality of parameter values comprise a style parameter value.

Claim 4 (original): The method of claim 1 wherein said plurality of parameter values comprises a bulk contact parameter value.

Claim 5 (currently amended): The method of claim 1 wherein ~~each of~~ said plurality of parameter values ~~is selected from the group consisting of~~ further comprise finger width, finger length, number of fingers, current, style, ~~slice,~~ and bulk contact parameter values.

Claim 6 (original): The method of claim 1 wherein said parasitic values of said at least one subcircuit model comprise a plurality of parasitic resistor values and a plurality of parasitic capacitor values.

Claim 7 (original): The method of claim 6 wherein said plurality of parasitic resistor values and said plurality of parasitic capacitor values are determined by said plurality of parameter values.

Claim 8 (original): The method of claim 6 further comprising a step of utilizing said plurality of resistor values and said plurality of capacitor values to simulate an electrical behavior of said multi-component circuit prior to said generating step.

Claim 9 (original): The method of claim 3 wherein said style parameter value determines how interconnect lines are routed in said layout of said multi-component circuit.

Claim 10 (original): The method of claim 4 wherein said bulk contact parameter value determines a location for bulk contacts in said layout of said multi-component circuit.

Claim 11 (currently amended): A method for designing a circuit block including at least one multi-component circuit, said multi-component circuit having at least one subcircuit model, said method comprising steps of:

receiving a plurality of parameter values for said at least one multi-component circuit, said plurality of parameter values comprising at least a slice parameter value;

determining a plurality of parasitic values for said at least one multi-component circuit;

simulating an electrical behavior of said circuit block utilizing said plurality of parasitic values;

generating a layout of said circuit block including said at least one multi-component circuit, said layout causing said at least one multi-component circuit to have said plurality of parasitic values.

Claim 12 (original): The method of claim 11 further comprising a step of performing a design rule check after said step of generating said layout.

Claim 13 (original): The method of claim 11 further comprising a step of performing a layout versus schematic verification after said step of generating said layout.

Claim 14 (original): The method of claim 11 further comprising a step of extracting interconnect parasitics after said step of generating said layout.

Claim 15 (original): The method of claim 11 wherein said plurality of parameter values comprise a style parameter value.

Claim 16 (original): The method of claim 11 wherein said plurality of parameter values comprises a bulk contact parameter value.

Claim 17 (currently amended): The method of claim 11 wherein each of said plurality of parameter values ~~is selected from the group consisting of~~further comprise finger width, finger length, number of fingers, current, style, ~~slice,~~ and bulk contact parameter values.

Claim 18 (original): The method of claim 11 wherein said parasitic values of said at least one subcircuit model comprise a plurality of parasitic resistor values and a plurality of parasitic capacitor values.

Claim 19 (original): The method of claim 18 wherein said plurality of parasitic resistor values and said plurality of parasitic capacitor values are determined by said plurality of parameter values.

Claim 20 (original): The method of claim 18 further comprising a step of utilizing said plurality of resistor values and said plurality of capacitor values to simulate an electrical behavior of said at least one multi-component circuit prior to said step of generating said layout.

Claim 21 (original): The method of claim 15 wherein said style parameter value determines how interconnect lines are routed in said layout of said at least one multi-component circuit.

Claim 22 (original): The method of claim 16 wherein said bulk contact parameter value determines a location for bulk contacts in said layout of said at least one multi-component circuit.

Claim 23 (currently amended): A system comprising a computer for designing a circuit block including at least one multi-component circuit, said at least one multi-component circuit having at least one subcircuit model, said computer implementing a method comprising steps of:

said computer receiving a plurality of parameter values for said at least one multi-component circuit in said circuit block, said plurality of parameter values comprising at least a slice parameter value;

said computer determining a plurality of parasitic values for said at least one multi-component circuit;

said computer generating a layout of said at least one multi-component circuit utilizing said plurality of parameter values, said layout causing said at least one multi-component circuit to have said plurality of parasitic values.

Claim 24 (original): The system of claim 23 wherein said method further comprises a step of said computer utilizing said plurality of parasitic values to simulate an electrical behavior of said at least one multi-component circuit prior to said step of said computer generating said layout.

Claim 25 (original): The system of claim 23 wherein said method further comprises a step of said computer performing a design rule check after said step of said computer generating said layout.

Claim 26 (original): The system of claim 23 wherein said method further comprises a step of said computer performing a layout versus schematic verification after said step of said computer generating said layout.

Claim 27 (original): The system of claim 23 wherein said method further comprises a step of said computer extracting interconnect parasitics after said step of said computer generating said layout.

Claim 28 (original): The system of claim 23 wherein said plurality of parameter values comprise a style parameter value.

Claim 29 (original): The system of claim 23 wherein said plurality of parameter values comprises a bulk contact parameter value.

Claim 30 (currently amended): The system of claim 23 wherein ~~each of~~ said plurality of parameter values ~~is selected from the group consisting of~~further comprise finger width, finger length, number of fingers, current, style, ~~slice,~~ and bulk contact parameter values.

Claim 31 (original): The system of claim 23 wherein said parasitic values of said at least one subcircuit model comprise a plurality of parasitic resistor values and a plurality of parasitic capacitor values.

Claim 32 (original): The system of claim 31 wherein said plurality of parasitic resistor values and said plurality of parasitic capacitor values are determined by said plurality of parameter values.

Claim 33 (original): The system of claim 28 wherein said style parameter value determines how interconnect lines are routed in said layout of said at least one multi-component circuit.

Claim 34 (original): The system of claim 29 wherein said bulk contact parameter value determines a location for bulk contacts in said layout of said at least one multi-component circuit.